REMARKS

Applicants have amended claims 2 and 11 to correct typographic errors. The amendment of claim 11 is not made in response to the Examiners rejection of claim 11.

The Examiner rejected claims 1-8, 10 under 35 U.S.C. §102(b) as being unpatentable over Noda (US 6,512,299).

The Examiner rejected claims 9 and 11 under 35 U.S.C. 103(a) as being unpatentable over Noda in view of Jung (US 6,335,279).

The Examiner rejected claims 12-18 under 35 U.S.C §112, (second paragraph) "as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention."

Applicants respectfully traverse the §112, §102(b) and §103(a) rejections with the following arguments.

35 USC § 112

As to claim 12, the Examiner states: "In claim 12, step (c), there is no antecedent basis for 'said first and second gates segments' , and 'gates' should be 'gate'. In step (d), there is no antecedent basis for 'said first PFET and said first NFET'. In step (d), there is no antecedent basis for 'said second PFET and said second NFET'." In response, Applicants have amended claim 12 to correct the antecedent basis of the first and second PFETs and the first and second NFETs.

As to claim 13, the Examiner states: "In claim 13, line 3, there is no antecedent basis for '"said sidewall layer'." In response, Applicants have amended both claim 12 and 13, to use the element "insulating sidewall layer."

As to claim 16, the Examiner states: "In claim 16, line 4, 'step (f) is performed after step (e)' is repeated and should be deleted." In response, Applicants have amended claim 16 to remove the second "step (f) is performed after step (e)' is repeated."

As to claim 17, the Examiner states: "In claim 17, line 3, there is no antecedent basis for 'said insulating capping layer'." In response, Applicants have changed the dependency of claim 17 from 16 to 12 in order to provide proper antecedent basis for "said insulating capping layer."

As to claim 18, the Examiner states: "In claim 18, line 10, '"secondPFET' should have a space between the words." In response, Applicants have corrected claim 18 as the Examiner has suggested.

35 USC § 102

As to claim 1, the Examiner states that "Noda (Figs. 2-3(f) and text in col. 5, line 1 to col. 6, line 8) discloses the claimed invention by forming a polysilicon line 22 with sidewalls, gate dielectric 13, insulating sidewalls 15, contacting doped silicon region 17, suicide layer 23."

Applicants contend that claim 1 is not anticipated by Noda because Noda does not teach each and every feature of claim 1. For example Noda does not teach "removing a portion of said polysilicon line."

Applicants respectfully point out that in Noda FIGs 1, 2 and 3(c) while SiO_2 spacers 15 are removed no portion of gate electrode 22 is removed and silicide layer 23 is formed over an intact gate electrode. Applicants respectfully point out that in Noda col. 5 line 1 to col. 6, line 8, that there is no mention of "removing a portion" of gate electrode 22.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Noda and is in condition for allowance. Since claims 2-11 depend from claim 1, Applicants respectfully maintain that claims 2-11 are likewise in condition for allowance.

35 USC § 103 Rejections

As to claim 11, the Examiner states that "Noda is applied as above and does not disclose the polysilicon doped N-type or P-type nor an insulating capping layer over the top surface of the polysilicon. Jung (Figs. 3C-3F and text in col. 6, line 15 to col. 7, line 12) teaches that polysilicon 108 is doped, and capping layer 112, which has been simultaneously removed with the polysilicon. It would have been obvious to one of ordinary skill in the art at the time the invention was made to dope the polysilicon as taught by Jung in Noda's process to form a conductive layer of the proper resistivity, and a capping layer to protect the lower layers and prevent current leakage."

Applicants contend that claim 11 is not obvious in view of Noda over Jung because Noda over Jung does not teach or suggest every feature of claim 11. For example, Noda over Jung does not teach or suggest "simultaneously removing corresponding sections of said insulating capping layer in said contact region of said polysilicon line." Applicants respectfully point out Jung teaches removing portions of an unpatterned blanket capping layer 112 and a unpatterned f blanket conductive layer 108 (FIG. 3C) with a single photoresist masking operation in order to form conductive pattern 116 and a capping layer pattern 120 (Parts of electrodes 118a and 118b of FIG. 3D). Since element 108 is an unpatterned blanket layer not a polysilicon line, Jung is not teaching removing a capping layer from a polysilicon line. Further, once conductive pattern 116 and capping layer pattern 120 are formed there is no teaching of removing a portion of capping layer pattern 120 from conductive pattern 116.

Based on the preceding arguments, Applicants respectfully maintain that claim 11 is not unpatentable over Nada over Jung and is in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Furukawa et al.

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BY: Jack P. Friedman
Jack P. Friedman
Reg. No. 44,688
FOR:
Anthony M. Palagonia
Registration No.: 41,237

3 Lear Jet Lane, Suite 201
Schmeiser, Olsen & Watts
Latham, New York 12110
(518) 220-1850
Agent Direct Dial Number: (802)-899-5460